

1.0A, 2.7V-15V Dual H-Bridge Motor Driver

Description

The SA8833C is a bipolar stepper-motor driver with dual, built-in full-bridges consisting of N channel power MOSFETs.

It operates from a supply voltage range of 2.7V to 15V and can deliver motor current up to 1.0A per channel. The internal safety features include overcurrent protection, short-circuit protection, sinking and sourcing current limits implemented with external sensors, under-voltage lockout and thermal shutdown. Internal An over-temperature output flag is available to indicate thermal shutdown.

The SA8833C is available in 5.0mm×6.4mm ETSSOP16L and QFN3X3-16 package.

Features

- Wide 2.7-15V Input Voltage Range
- Continuous current up to 1.0A
- $R_{DS(on)}$: 950mΩ (HS+LS)
- Low Quiescent Current
- Low Sleep Current
- Thermal Shutdown protection
- Under-Voltage Lockout Protection
- Over-Current Protection
- Over-Temperature Output Flag
- PWM Winding Current Regulation and Current Limiting
- ETSSOP16L, QFN3X3-16 Package

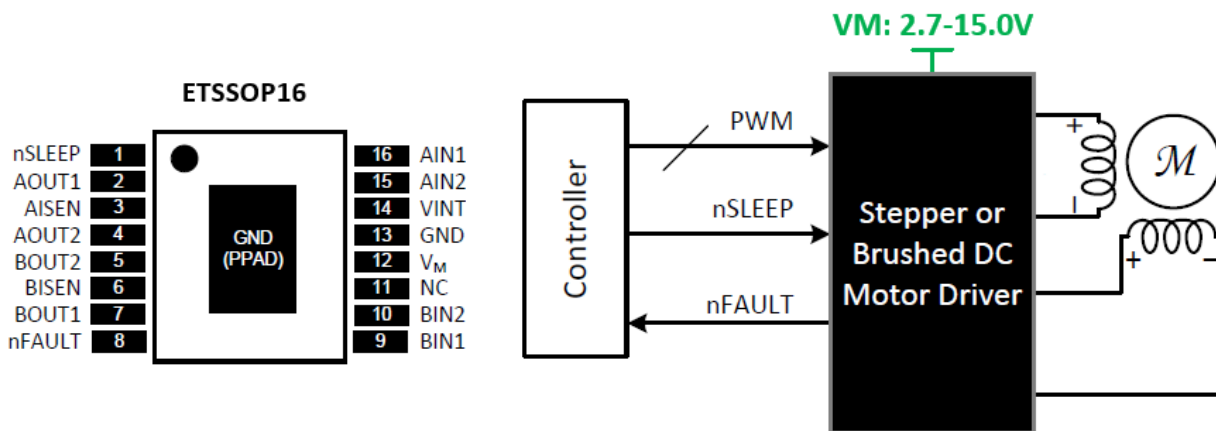
Applications

- POS Printers
- Video Security Camera
- Digital Still Cameras
- Battery Powered Toys

Device Information

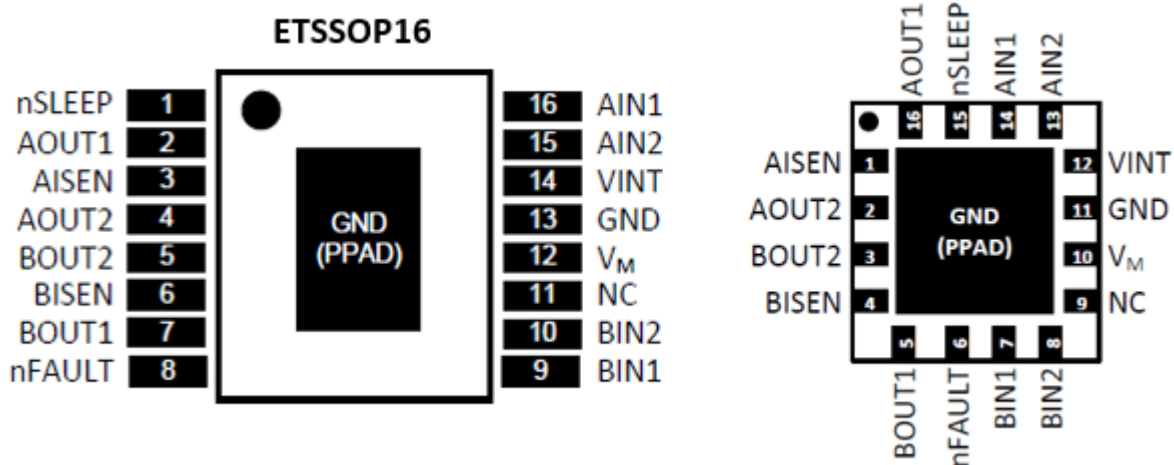
Part No.	Package	Quantity
SA8833C	ETSSOP16L	4000/Reel
SA8833C	QFN3X3-16	4000/Reel

SA8833C Simplified Schematic



1.0A, 2.7V-15V Dual H-Bridge Motor Driver

Pin Descriptions



NAME	ETSSOP16L	QFN3X3-16	TYPE	DESCRIPTION
nSleep	1	15	P	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
AOUT1	2	16	O	Bridge A output 1
AISEN	3	1	O	Sense resistor to GND sets PWM current regulation level
AOUT2	4	2	O	Bridge A output 2
BOUT2	5	3	O	Bridge B output 2
BISEN	6	4	O	Sense resistor to GND sets PWM current regulation level
BOUT1	7	5	O	Bridge B input 1
nFAULT	8	6	O	Pulled logic low with fault condition; open-drain output requires an external pullup
BIN1	9	7	I	Bridge B input 1
BIN2	10	8	I	Bridge B input 2
NC	11	9	NC	No Connection
VM	12	10	P	Connect to motor supply voltage; bypass to GND with a 10-uf (minimum) capacitor rated for VM
GND	13	11	P	Both the GND pin and device PowerPAD must be connected to ground
VINT	14	12		Internal supply voltage
AIN2	15	13	I	Bridge A input 2
AIN1	16	14	I	Bridge A input 1

1.0A, 2.7V-15V Dual H-Bridge Motor Driver
Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

Parameter		Min.	Max.	Unit
Power Supply	VM	-0.3	16.5	V
Input Logic	Digital input pin voltage	-0.3	7.0	V
xISEN	Xsen pin voltage	-0.3	0.5	V
Peak current of output	I _{OUTA_PEAK} , I _{OUTB_PEAK}	Internal limited		A
ESD(HBM)		2.0		kV
Operation temp.	T _J	-40	150	°C
Storage temp.	T _{stg}	-65	150	°C
Thermal resistance	ETSSOP16 θ_{JA}		75	°C/W

Recommended operating conditions ($T_A=25^{\circ}\text{C}$)

Parameter		Min.	Max.	Unit
Power Supply	VM	2.7	15.0	V
Input Logic	Digital input pin voltage	0	5.5	V
f _{PWM}	Applied PWM signal to AIN1,AIN2,BIN1,BIN2	0	200	kHz
Output Contiguous Current	I _{OUTA} , I _{OUTB}	0	1.0*	A

Notes: * Using 25mm² FR4 Signal layer PCB (1 oz) under VM=7.2V test.

1.0A, 2.7V-15V Dual H-Bridge Motor Driver
Electrical Characteristics (V_M=7.4V, T_A=25 °C, R_{LOAD}=20)

over operating free-air temperature range (unless otherwise noted)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power Supply					
VM operating voltage	VM	2.7		15	V
VM operating supply current	I _{VM_ON}	VM=5.0V	1.0	2.0	mA
VM sleep mode supply current	I _{VM_OFF}	Nsleep=0	1.0	2.5	uA
Wake-up time	t _{WAKE}		70		us
Internal regulator voltage	V _{INT}		5.0		V
H-Bridge FETs					
ON Resistance, HS+LS	R _{DSON}	VM=2.7V, I _{OUT} =0.2A	1250		mΩ
		VM=5.0V, I _{OUT} =0.2A	950		mΩ
		VM=7.4V, I _{OUT} =0.2A	950		mΩ
Off-state leakage current	I _{OFF}	VM=5.0V	-1	1	uA
Output rise time	t _{RISE}		250		ns
Output fall time	t _{FALL}		150		ns
Propagation Delay Time (On)	t _{ON_DELAY}	INx high to OUTx on	1050		ns
Propagation Delay Time (Off)	t _{OFF_DELAY}	INx low to OUTx off	650		ns
Output dead time	t _{DEAD}		300		ns
PWM CURRENT CONTROL (AISEN, BISEN)					
xISEN trip voltage	V _{TRIP}		200		mV
Blanking time	t _{BLANK}		2.0		us
Current control constant off time	t _{OFF}	Internal PWM constant off time	20		us
AIN1, AIN2, BIN1, BIN2, nSLEEP					
Input high level voltage	V _{IH}	nSLEEP	2.0		V
	V _{IH}	All otherpins	2.5		V
Input low level voltage	V _{IL}	nSLEEP	0	0.5	V
	V _{IL}	All otherpins		0.7	V
Pull down resistance	R _{PD}		200		KΩ
CONTROL OUTPUTS (nFAULT)					
Output logic low voltage	V _{OL}	I _O =5mA		0.5	V
Output logic high leakage	I _{OH}		0	1	uA

1.0A, 2.7V-15V Dual H-Bridge Motor Driver

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Condition	Min.	Typ.	Max.	Unit
PROTECTION CIRCUITS						
VM undervoltage lockout	V _{UVLO_R}	VM rising			2.7	V
	V _{UVLO_F}	VM falling			2.6	V
VM undervoltage hysteresis	V _{UVLO_H}			100		mV
Overcurrent protection trip level	I _{OCP}			2.0		A
Overcurrent deglitch time	t _{DEG}			1.6		us
Overcurrent protection period	t _{OCP}			1.0		ms
Thermal shutdown protection	T _{OTSD}			160		°C
Thermal shutdown hysteresis	T _{HYS}			35		

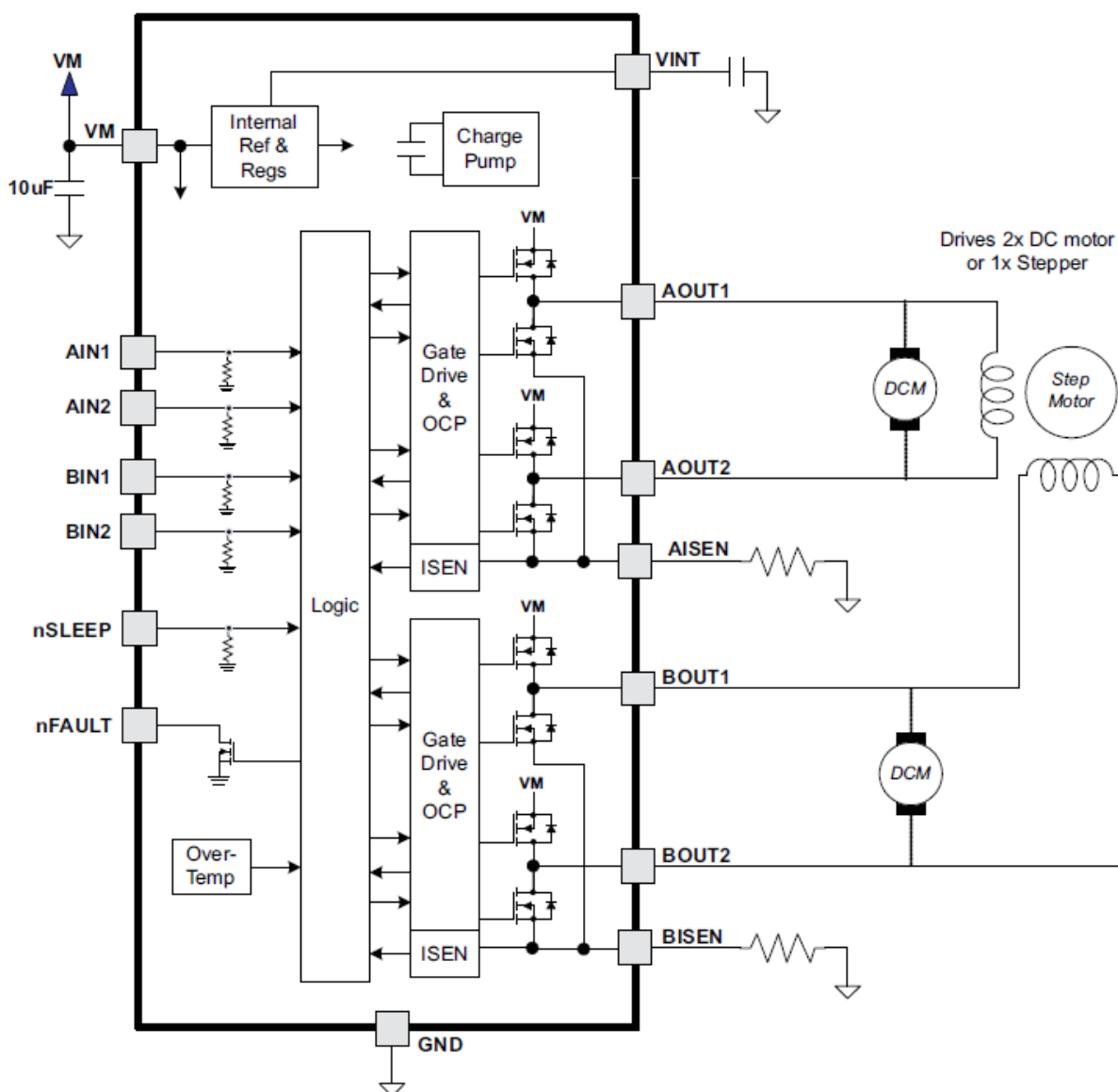
1.0A, 2.7V-15V Dual H-Bridge Motor Driver

Application Notes:

The SA8833C device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two NMOS H-bridges. The SA8833C can be powered with a supply voltage from 2.7 to 15V and can provide an output current up to 1.0A.

The motor output current can be controlled by an external pulse width modulator (PWM) current controller. The SA8833C includes a lower power sleep mode, which lets the system save power when not driving the motor.

1. Function Block Diagram



1.0A, 2.7V-15V Dual H-Bridge Motor Driver

2. EXTERNAL PWM CURRENT CONTROL

SA8833C contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 1 shows a block diagram of circuitry.

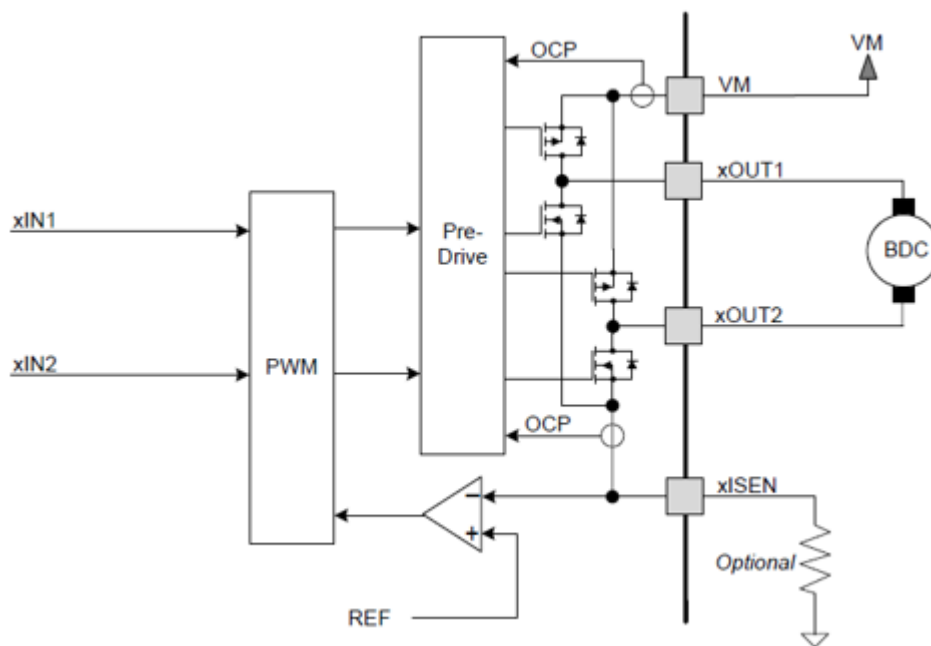


Figure 1. Motor Control Circuitry

3. Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs. Table 1 shows the logic.

Table 1. H-Bridge Logic

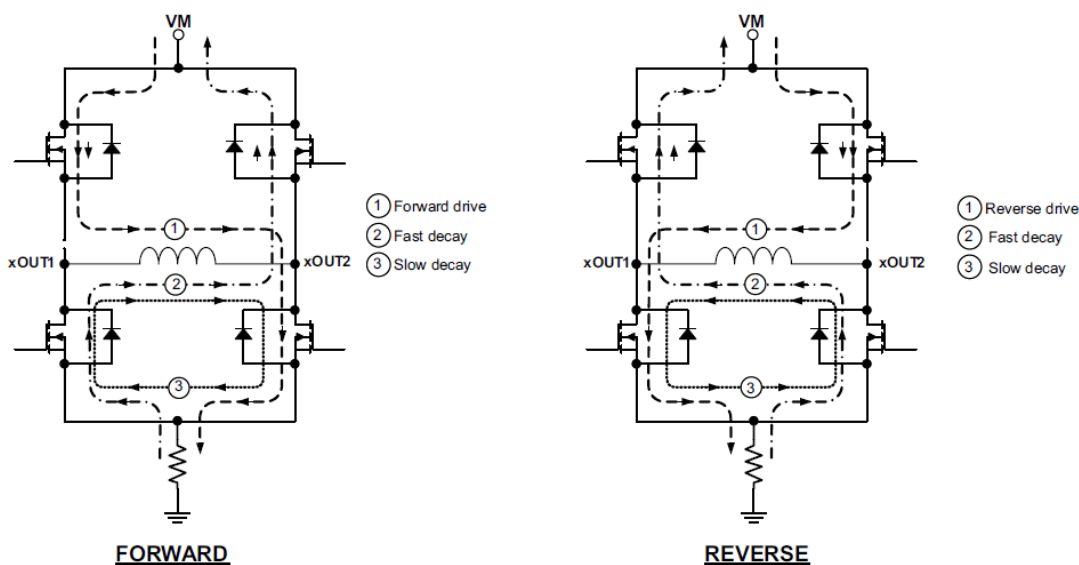
xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast/fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/slow decay

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states: fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted. To PWM using fast decay, the PWM signal is applied to one xIN pin while the other is held low; to use slow decay, one xIN pin is held high.

1.0A, 2.7V-15V Dual H-Bridge Motor Driver
Table 2. PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

The internal current control is still enabled when applying external PWM to xIN. To disable the current control when applying external PWM, the xISEN pins should be connected directly to ground. [Figure 2](#) show the current paths in different drive and decay modes.


Figure 2. Drive and Decay Modes

4. Current Control

The current through the motor windings may be limited, or controlled, by a 20- μ s constant off-time PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Note that immediately after the output is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 2.0 μ s.

The PWM chopping current is set by a comparator that compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage, V_{TRIP} , is fixed at 200 mV nominally.

1.0A, 2.7V-15V Dual H-Bridge Motor Driver

The chopping current is calculated as in [Equation 1](#).

$$I_{CHOP} = \frac{200mV}{R_{XISEN}} \quad (1)$$

Example: If a 1-Ω sense resistor is used, the chopping current will be 200 mV / 1 Ω = 200 mA.

5. Decay Mode

After the chopping current threshold is reached, the H-bridge switches to slow-decay mode. This state is held for t_{OFF} (20 μs) until the next cycle to turn on the high-side MOSFETs.

6. Slow Decay

In slow-decay mode, the high-side MOSFETs are turned off and both of the low-side MOSFETs are turned on. The motor current decreases while flowing in the two low-side MOSFETs until reaching its fixed off time (typically 20 μs). After that, the high-side MOSFETs are enabled to increase the winding current again.

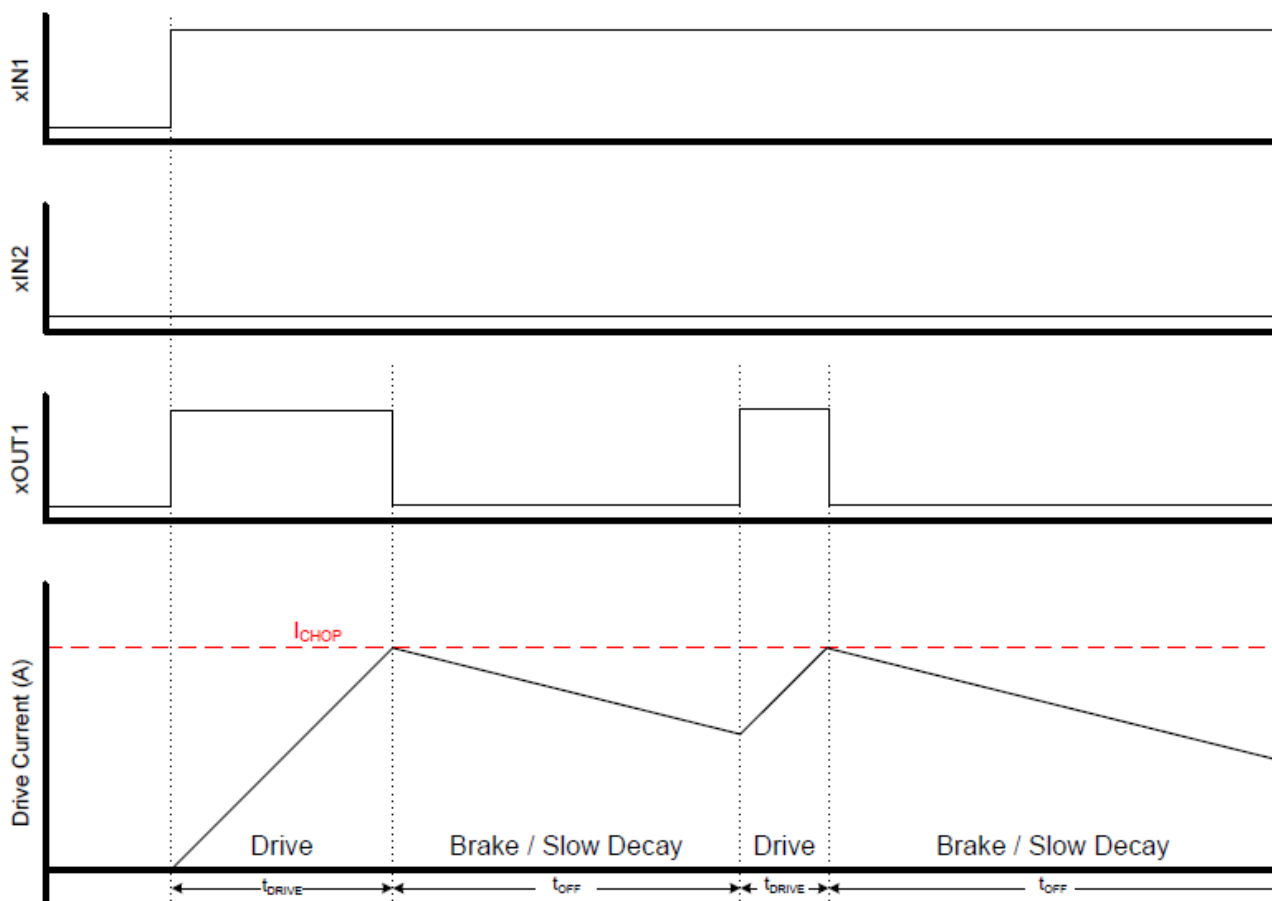


Figure 3. Current Chopping Operation

1.0A, 2.7V-15V Dual H-Bridge Motor Driver

7. Sleep Mode

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time, t_{WAKE} , needs to pass before the motor driver becomes fully operational. To make the board design simple, the nSLEEP can be pulled up to the supply (VM). It recommends to use a pullup resistor when this is done. This resistor limits the current to the input in case VM is higher than 6.5V. Internally, the nSLEEP pin has a 200kΩ resistor to GND. It also has a clamping Zener diode that clamps the voltage at the pin at 6.5 V. Currents greater than 250 μA can cause damage to the input structure. Therefore, It recommends a pullup resistor between 20 to 75 kΩ.

8. Parallel Mode

The two H-bridges in the SA8833C can be connected in parallel for double the current of a single H-bridge. The internal dead time in the SA8833C prevents any risk of cross-conduction (shoot-through) between the two bridges due to timing differences between the two bridges. [Figure 4](#) shows the connections.

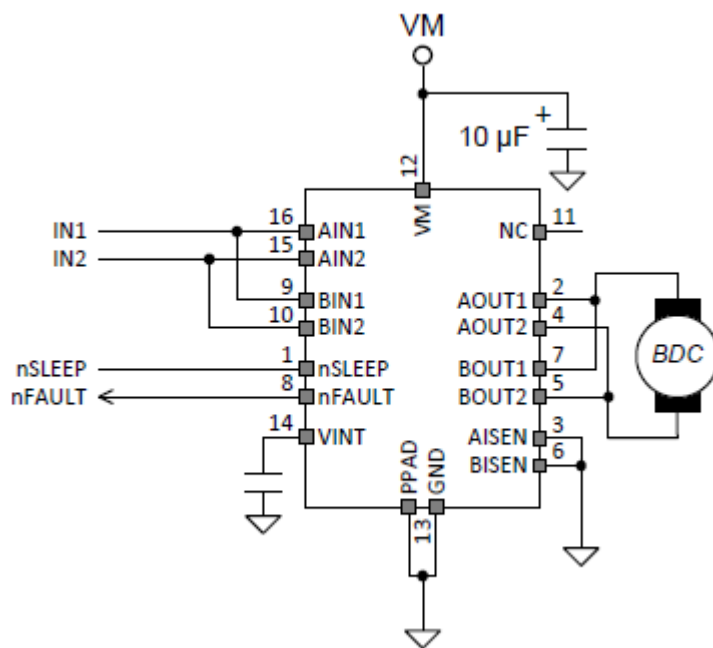


Figure 4. Parallel Mode Schematic

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9. Protection Circuits

The SA8833C is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time, all FETs in the H-bridge will be disabled. The driver will be re-enabled after the OCP retry period (t_{OCP}) has passed. If the fault condition is still present, the cycle repeats. Overcurrent conditions are detected independently on both high- and low-side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for PWM current control.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. Once the die temperature has fallen to a safe level, operation will automatically resume.

Undervoltage Lockout (UVLO)

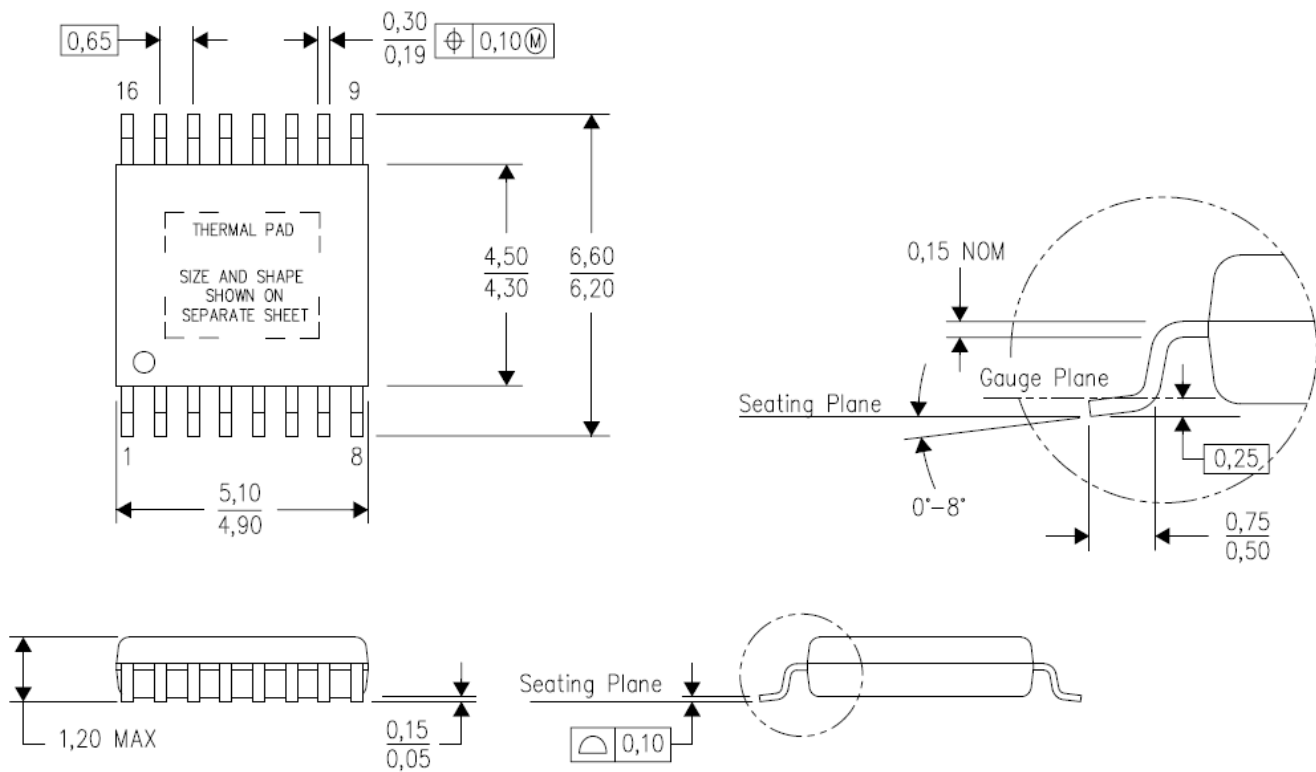
If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

Table 3. Device Protection

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < 2.5\text{ V}$	None	Disabled	Disabled	$V_M > 2.7\text{ V}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	FAULTn	Disabled	Operating	OCP
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	FAULTn	Disabled	Operating	$T_J < T_{TSD} - T_{HYS}$

1.0A, 2.7V-15V Dual H-Bridge Motor Driver

Package ETSSOP16L



1.0A, 2.7V-15V Dual H-Bridge Motor Driver

QFN3X3-16

